IN THE CLAIMS:

Please cancel claim 4 without prejudice to or disclaimer of the subject matter recited therein.

Please amend claim 1 as follows:

LISTING OF CURRENT CLAIMS

1. (Currently Amended) A speed-up hardware architecture used in wireless encryption/decryption operation, comprising:

a plurality of advance encryption standard (AES) operation units, ~~that each operation unit~~ each of the plurality of advance encryption standard (AES) operation units is capable of accomplishing a designated advance encryption standard (AES) operation independently, ~~further~~ and comprising:

a data receiving device having two inputs that a first input is used for receiving an external data signal and a second input is used for receiving a supporting signal coming from the other operation unit, wherein, when an operating mode of the data receiving device is "normal", the data receiving device will output the first input, and when an operating mode of the data receiving device is "speed-up", the data receiving device will output the second input; and

an operating device coupling to the data receiving device for processing data from the data receiving device and outputting the processed data thereafter; and

a control unit coupling to every operation unit in the architecture for enabling operation units which are idle to assist working operation units for data processing, further comprising:

a controlling device coupling to the data receiving device of every operation unit in the architecture for issuing a control signal and changing the operating mode; and

an integrating device coupling to the operating device of every operation unit in the architecture for integrating outputs coming from the operating devices of the operation units which are in "speed-up mode".

2. (Original) The speed-up hardware architecture of claim 1, wherein the data receiving device is a multiplexer.

3. (Original) The speed-up hardware architecture of claim 1, wherein the data receiving device is a double word selection logic.

Claim 4. (Canceled)

5. (Original) The speed-up hardware architecture of claim 1, wherein the architecture comprises two AES operation units.

6. (Original) The speed-up hardware architecture of claim 1, wherein the controlling device is further connected to the operating device of every operation unit in the architecture for detecting if the operating device is idle.

7. (Original) The speed-up hardware architecture of claim 1, wherein the controlling device is able to transmit data.

8. (Original) The speed-up hardware architecture of claim 1, wherein the integrating device can be connected directly to the operating device of another operation unit for accessing the output thereof directly.